Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An arrangement for interconnection of two or more printed circuit boards communicating with each other over a time division multiplex data bus, each circuit board including a number of loads transferring data in both a receive and transmit direction, comprising:

a local time division multiplex data bus in each printed circuit board to which the associated number of loads are connected,

an intermediate Central Processing Unit controlled logic in each direction connecting each local time division multiplex data bus to a global time division multiplex data bus, which is a back plane time division multiplex data bus, said arrangement being implemented in a circuit switched node , and said control logic including: ~~which logic includes~~

a First-In-First-Out buffer through which synchronous data from the respective local time division multiplex data bus or the global time division multiplex data bus is being written in and read out to the respective local time division multiplex data bus or the global time division multiplex data bus introducing a phase difference, providing a total delay for any data traveling from the respective local time division multiplex data bus to the global time division multiplex data bus and back to the respective local time division multiplex data bus, being of a controllable dimension equal to an integer number of data frames; and

a first and a second time slot counter, the first counter addressing a first data location in the First-In-First-Out buffer into which, in case of receive direction, time slot data from a local time division multiplex data bus is to be written, or out of which, in case of transmit direction, time slot data to a local time division multiplex bus is to be read, the second counter addressing a second data

location in the First-In-First-Out buffer into which, in case of transmit direction, time slot data from the global time division multiplex bus is to be written, or out of which, in case of receive direction, time slot data to the global time division multiplex bus is to be read, wherein the phase difference between the first and the second time slot counter represents a preferred part of said total delay caused by the logic of the respective direction.

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2. – 3. (Canceled)

4. (Currently Amended) The arrangement as defined in claim 1 [[3]], wherein the first counter is incremented by a first clock corresponding to the current local time division multiplex data bus and initialised by a first frame synchronisation signal indicating the start of each frame in the current local time division multiplex data bus, the second counter is incremented by a second clock corresponding to the global time division multiplex data bus and initialised by a second frame synchronisation signal indicating the start of each frame in the global time division multiplex data bus.

5. (Previously Presented) The arrangement as defined in claim 4, wherein the first clock and frame synchronisation signal is derived from the second clock and frame synchronisation signal, adapted to provide said preferred part of said total delay caused by the logic of the respective direction.

6. (Currently Amended) The arrangement as defined in claim 1 [[3]], wherein the logic further includes a table including one bit per data location in the First-In-First-Out buffer, wherein, in case of transmit direction, if a first logic value is assigned to the data location addressed by the first counter, reading of the content in that data location to the certain local time division multiplex data bus is enabled, in contrast to a second logic value in which case reading is disabled, and in case of receive direction, if a first logic value is assigned to the data location addressed by the second counter.

reading of the content in that data location to the global time division multiplex data bus is enabled, in contrast to a second logic value in which case reading is disabled.

7. (Currently Amended) The arrangement as defined in claim 1 [[3]], wherein the preferred part of said total delay caused by the logic of the receive direction is the duration of one frame minus the preferred part of said total delay caused by the logic of the transmit direction.

8. (Previously Presented) The arrangement as defined in claim 7, wherein the preferred part of said total delay caused by the logic of the transmit direction is the duration of 8 or 16 time slots.

9. (Previously Presented) The arrangement as defined in claim 1, wherein the circuit switched node is a Base Station Controller or a switch in any circuit switched enabled data or telecommunication network.